This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-4. (canceled)

5. (currently amended): A method for designing an integrated circuit, comprising:

manipulating representations of components of an integrated circuit on a display device by a user;

specifying an interconnect having at least one of a communication characteristic and a performance characteristic between a first represented component and a second represented component; and

extracting data suitable for describing the specified interconnect between the first represented component and the second represented component;

wherein the extracted data includes a direct connectivity definition.

6. (canceled)

7. (previously presented): A method for designing an integrated circuit, comprising:

manipulating representations of components of an integrated circuit on a display device by a user;

specifying an interconnect having a characteristic between a first represented component and a second represented component; and

extracting data suitable for describing the specified interconnect between the first represented component and the second represented component;

wherein the specified characteristic includes at least one of bandwidth, latency and scalability.

8. (canceled)

9. (previously presented): A method for designing an integrated circuit, comprising:

manipulating representations of components of an integrated circuit on a display device by a user;

specifying an interconnect having a characteristic between a first represented component and a second represented component;

extracting data suitable for describing the specified interconnect between the first represented component and the second represented component; and

optimizing at least one of the components and interconnects;

wherein optimizing includes at least one of arranging components of the integrated circuit and specifying bandwidth between components.

10. (original): The method as described in claim 9, wherein components are arranged based on latency, scalability, timing considerations, power considerations, data switching and bandwidth.

11. (previously presented): A method for designing an integrated circuit, comprising:

manipulating representations of components of an integrated circuit on a display device by a user;

specifying an interconnect having a characteristic between a first represented component and a second represented component;

extracting data suitable for describing the specified interconnect between the first represented component and the second represented component; and

optimizing at least one of the components and interconnects;

wherein optimizing is performed without user intervention by an agent.

12. (canceled)

13. (previously presented): A method for designing an integrated circuit, comprising:

manipulating representations of components of an integrated circuit on a display device by a user;

specifying an interconnect having a characteristic between a first represented component and a second represented component; and

extracting data suitable for describing the specified interconnect between the first represented component and the second represented component;

wherein components include standardized interfaces.

14. (previously presented): The method as described in claim 13, wherein the standardized interfaces communicate over interscalable, isochronous interconnect glue logic.

15. (previously presented): A method for designing an integrated circuit, comprising:

manipulating representations of components of an integrated circuit on a display device by a user;

specifying an interconnect having a characteristic between a first represented component and a second represented component; and

extracting data suitable for describing the specified interconnect between the first represented component and the second represented component;

wherein interconnects not specified by a user are automatically configured by an agent.

16. (canceled)

17. (previously presented): A system for designing an integrated circuit, comprising:

a display device, the display device suitable for displaying representations of components of an integrated circuit for manipulation by a user;

a memory suitable for storing a program of instructions; and

a processor suitable for performing the program of instructions, the processor communicatively coupled to the display device and the memory, wherein the program of instructions configures the processor to

display representations of components of an integrated circuit for manipulation by a user on the display device so that a user may specify an interconnect having a characteristic between a first component representation and a second component representation, and

extract data describing the first represented component, the second represented component and the specified interconnect as manipulated by the user;

wherein the specified characteristic includes at least one of bandwidth, scalability and latency.

18. (currently amended): The system as described in claim 17, wherein ~~bandwidth is~~ the scalability specified ~~including~~ includes at least one of number of links and speed of links.

19-21. (canceled)

22. (previously presented): A system for designing an integrated circuit, comprising:

a display device, the display device suitable for displaying representations of components of an integrated circuit for manipulation by a user;

a memory suitable for storing a program of instructions; and

a processor suitable for performing the program of instructions, the processor communicatively coupled to the display device and the memory, wherein the program of instructions configures the processor to

display representations of components of an integrated circuit for manipulation by a user on the display device so that

a user may specify an interconnect having a characteristic between a first component representation and a second component representation, and

extract data describing the first represented component, the second represented component and the specified interconnect as manipulated by the user;

wherein interconnects not specified by a user are automatically configured by an agent.

23. (canceled)

24. (previously presented): A system for designing an integrated circuit, comprising:

a display device, the display device suitable for displaying representations of components of an integrated circuit for manipulation by a user;

a memory suitable for storing a program of instructions;

a processor suitable for performing the program of instructions, the processor communicatively coupled to the display device and the memory, wherein the program of instructions configures the processor to

display representations of components of an integrated circuit for manipulation by a user on the display device so that a user may specify an interconnect having a characteristic between a first component representation and a second component representation; and

extract data describing the first represented component, the second represented component and the specified interconnect as manipulated by the user;

and

an integrated circuit communicatively coupled to the processor, wherein the integrated circuit receives the extracted data, wherein the extracted data is utilized by the integrated circuit for being programmed to

include the interconnect having the characteristic between a first component corresponding to the first component representation and a second component corresponding to the second component representation;

wherein the specified characteristic includes at least one of bandwidth, latency and scalability.

25. (currently amended): The system as described in claim 24, wherein ~~bandwidth~~ the scalability specified ~~including~~ includes at least one of number of links and speed of links.

26-27. (canceled)

28. (previously presented): A system for designing an integrated circuit, comprising:

a display device, the display device suitable for displaying representations of components of an integrated circuit for manipulation by a user;

a memory suitable for storing a program of instructions;

a processor suitable for performing the program of instructions, the processor communicatively coupled to the display device and the memory, wherein the program of instructions configures the processor to

display representations of components of an integrated circuit for manipulation by a user on the display device so that a user may specify an interconnect having a characteristic between a first component representation and a second component representation; and

extract data describing the first represented component, the second represented component and the specified interconnect as manipulated by the user;

and

an integrated circuit communicatively coupled to the processor, wherein the integrated circuit receives the extracted data, wherein the extracted data is utilized by the integrated circuit for being programmed to include the interconnect having the characteristic between a first component corresponding to the first component representation and a second component corresponding to the second component representation;

wherein interconnects not specified by a user are automatically configured by an agent.

29-30. (canceled)

31. (previously presented): An application specific integrated circuit, comprising:

a first component suitable for providing an integrated circuit function, the first component communicatively coupled to a first interface device;

a second component suitable for providing an integrated circuit function, the second component communicatively coupled to a second interface device;

an interconnect suitable for communicatively coupling the first interface device with the second interface device so as to enable communication of the first component with the second component;

a memory suitable for storing a program of instructions, the program of instructions including data received for configuring an interconnect having a characteristic between components of an application specific integrated circuit; and

a microprocessor suitable for performing the program of instructions, the microprocessor communicatively coupled to the memory, wherein the program of instructions configures the microprocessor to configure the first component, the second component, and the interconnect to correspond to an interconnect having the characteristic as indicated by the program of instructions;

wherein the interconnect is interscalable.

32. (canceled)

33. (previously presented): An application specific integrated circuit, comprising:

a first component suitable for providing an integrated circuit function, the first component communicatively coupled to a first interface device;

a second component suitable for providing an integrated circuit function, the second component communicatively coupled to a second interfa ce device;

an interconnect suitable for communicatively coupling the first interface device with the second interface device so as to enable communication of the first component with the second component;

a memory suitable for storing a program of instruc tions, the program of instructions including data received for configuring an interconnect having a characteristic between components of an application specific integrated circuit; and

a microprocessor suitable for performing the program of instructions, the microprocessor communicatively coupled to the memory, wherein the program of instructions configures the microprocessor to configure the first component, the second component, and the interconnect to correspond to an interconnect having the characteristic as indicated by the program of instructions;

wherein the microprocessor is suitable for self-programming to enable optimization of the ASIC, and

wherein optimization includes routing of packeted data.

34. (previously presented): An application specific integrated circuit, comprising:

a first component suitable for providing an integrated circuit function, the first component communicatively coupled to a first interface device;

a second component suitable for providing an integrated circuit function, t he second component communicatively coupled to a second interface device;

an interconnect suitable for communicatively coupling the first interface device with the second interface device so as to enable communication of the first component with the secon d component;

a memory suitable for storing a program of instructions, the program of instructions including data received for configuring an interconnect having a characteristic between components of an application specific integrated circuit; and

a microprocessor suitable for performing the program of instructions, the microprocessor communicatively coupled to the memory, wherein the program of instructions configures the microprocessor to configure the first component, the second component, and the interconnect to correspond to an interconnect having the characteristic as indicated by the program of instructions;

wherein packeted data is routed based on at least one of an indicated priority of data, component resource availability, priority of data when compared through use of heuristic data and data characteristic.

35. (original): The application specific integrated circuit as described in claim 34, wherein the data characteristic includes streaming data and electronic storage device data.

36. (original): The application specific integrated circuit as described in claim 34, wherein component resource availability is determined by at least one of an amount of data previously transferred to a component, amount of data received from the component, characteristic of data sent to the component and characteristic of data received from the component.